

Attorney Docket No. 23600.01901
Client Ref. No. 01900

UNITED STATES PATENT APPLICATION FOR:

**COMMUNICATION RECEIVER WITH SIGNAL PROCESSING
FOR BEAM FORMING AND ANTENNA DIVERSITY**

Inventor:
Hillel Hendler

COMMUNICATION RECEIVER WITH SIGNAL PROCESSING
FOR BEAM FORMING AND ANTENNA DIVERSITY

5

Inventor:
Hillel Hendler

10

15

COPYRIGHT NOTICE

20

A portion of the disclosure of this patent document contains material which is subject to copyright protection. The copyright owner has no objection to the facsimile reproduction by anyone of the patent document or the patent disclosure, as it appears in the Patent and Trademark Office patent file or records, but otherwise reserves all copyright rights whatsoever.

25

30

Cross Reference To Related Applications and Claim of
Priority

This invention claims priority to the following co-pending U.S. provisional patent application, which is incorporated herein by reference, in its entirety:

35

Hendler, Provisional Application Serial No.
60/189,329, entitled "COMMUNICATION RECEIVER WITH SIGNAL

PROCESSING FOR BEAM FORMING AND ANTENNA DIVERSITY,"
attorney docket no. 23600.01900, filed, 14 March, 2000.

5

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to wireless
communication receivers, and amongst other things to
10 wireless communication receivers having signal processing
capability for performing beam forming, antenna diversity,
as well as other functions.

15

Discussion of Background

Wireless modems are used to interconnect computers or
LANs using radio waves. Radio signals have advantages and
disadvantages over hardwire systems. The wireless
20 advantages include quick deployment, higher data rates than
conventional telephone lines and the ability to serve
customers independently of the traditional infrastructure.

The disadvantages of wireless transmission in the
range of the MMDS/ITFS (multi-channel multi-point

distribution system/instructional television fixed service) channels include fading and multi-path.

Wireless receivers utilize several techniques to overcome channel impairments like fading and multi-path.

5 Once class of techniques to reduce fading and multi-path are referred to as beam forming. Beam forming techniques increase the antenna gain, and more importantly increases the antenna directivity while also allowing controllable direction selectivity. This enables reduction of external
10 interference and improvement of the robustness against multi-path.

Another class of techniques to reduce problems associated with fading and multi-path are referred to as antenna diversity. Antenna diversity uses two or more
15 antennas that are shifted in space by one or more wavelengths of the transmitted carrier frequency. The spatial shifting can influence and many times it reduces fading. Diversity involves downconverting and demodulating the received signal in parallel from the two or more
20 antennas and then selecting the "best" signal by post detection decision criteria.

Referring to Fig. 1, a common technique used for antenna diversity in wireless systems is depicted. Each of

the two antennas 5 and 10 is connected to a separate full channel receiver which includes a low noise amplifier (LNA) 15 and 20, a down converter 25 and 30, and a demodulator decoder 35 and 40. The demodulator decoders 30 and 40 each receive an analog signal either at an IF or a baseband frequency and then demodulate the analog signal to provide a digital signal which has also been error corrected. After decoding and error correcting the digital signal each demodulator decoder 30 and 40 delivers a decoded data stream, comprising data packets, along with error information related to each data packet of the digital signal. The digital signal from each of the demodulators 30 and 40 is delivered to the buffer 50, while the error information is delivered to diversity controller 45. The diversity controller 45 selects the best packet data stream from the one of the two demodulators 35 or 45 according to a predetermined minimum error criterion. The selected data packet is then provided at data output 55.

Referring to Fig. 2, a known technique used for beam forming in wireless receivers is depicted. The system of Fig. 2 utilizes vector combining, of amplitude and phase, of the signal received by each of two antennas 110 and 115. By amplitude balancing and adjusting the phase of the

relative signals a shift in the direction of the combined antenna beam is achieved. The two received signals are typically combined in a beam forming RF module 80 that operates at the transmitted RF frequency. The signals from

5 each of the two antennas 110 and 115 after been amplified by the attached low noise amplifier 70 and 75 is delivered to the beam forming module 80. The beam-forming module 80 includes a phase shift and amplitude control unit 85 and a RF combiner 90. The combined signal output by combiner 90

10 is a standard received signal at RF. The combined signal is then provided to a downconverter 95 and then to analog to digital converter (A/D) 100. The digital signal is provided to a demodulator 105 with a channel estimation capability. The demodulator 105 utilizes the estimation

15 capability to control the beam forming RF module for optimization of the received signal and for error minimization. The two antenna elements as described in Fig. 2 are very common for low cost wireless applications, but the same concept can be used with more antennas.

20 Therefore, the beam-forming scheme depicted in Fig. 2 can be implemented with two antennas or with a phased array.

The techniques described with respect to Figs. 1 & 2 require a full receiving chain for each antenna. This is

both expensive and increases the potential points of failure in a wireless receiver.

SUMMARY OF THE INVENTION

5 The present invention provides a technique to reduce the number of RF components by using digital signal processing functions in wireless receivers having two or more antennas, which results in the reduction of system cost. The reduction occurs by using an RF multiplexer or
10 RF switch to sample the signal received by each of the antennas. By sampling the RF signal from the two (or more) antennas, the invention enables to implement a single RF chain, instead of dual (or more) RF chains in a conventional implementation of beam forming or antenna
15 diversity. The sampling rate of the multiplexer or switch is greater than the Nyquist required sampling rate (F_s) of the received signal bandwidth. The sampled signal is a multiplexed single analog (RF) signal, which only requires one chain of receiver components. A signal processor then
20 is able to demultiplex the received signal at a lower frequency and can perform several functions including antenna diversity and beam forming utilizing digital signals at IF or baseband frequencies. The present

invention may also be applied to signals other than RF, including, but not limited to, High Frequency (HF) signals, Microwave, x-ray, optical, laser, or other signal types.

In one embodiment the present invention provides for a
5 wireless communication receiver comprising at least two
antennas each configured to receive a communication signal,
a switch coupled to the at least two antennas and that
provides a multiplexed signal, a downconverter that
provides a downconverted multiplexed signal, and a signal
10 processor that receives the downconverted signal and that
provides a data signal.

In an additional embodiment, the present invention
provides for a method for receiving a communication signal
at a wireless communication device comprising at least two
15 antennas. The method comprises receiving at each of at
least two antennas a communication signal, sampling the
communication signal to produce a sampled signal, down
converting the sampled signal to generate a down converted
signal, generating a digitized signal from the down
20 converted signal, and demultiplexing the digitized signal
to produce at least two digital signals each corresponding
to the communication signal as received by the at least two
antennas.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily
5 obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

Fig. 1 is a block diagram of a known antenna diversity scheme for a wireless receiver;

10 Fig. 2 is a block diagram of a known beam-forming scheme for a wireless receiver;

Fig. 3 is a block diagram of a presently preferred embodiment of an antenna diversity and beam forming wireless communication receiver according to the present
15 invention;

Fig. 4 is a block diagram of a presently preferred embodiment of a beam forming signal processor according to the present invention; and

Fig. 5 is a block diagram of a presently preferred
20 embodiment of an antenna diversity signal processor according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a technique to reduce the number of RF components by using digital signal processing functions in wireless receivers having two or more antennas, which results in the reduction of system cost. By sampling the RF signal from the two (or more) antennas, the invention enables to implement a single RF chain, instead of dual (or more) RF chains in a conventional implementation of beam forming or antenna diversity. The reduction occurs by using an RF multiplexer or RF switch to sample the signal received by each of the antennas. The sampling rate of the multiplexer or switch is greater than the Nyquist required sampling rate (F_s) of the received signal bandwidth. The sampled signal is a multiplexed single analog (RF) signal, which only requires one chain of receiver components. A signal processor then is able to demultiplex the received signal at a lower frequency and can perform several functions including antenna diversity and beam forming utilizing digital signals at IF or baseband frequencies.

Referring again to the drawings, wherein like reference numerals designate identical or corresponding parts, and more particularly to Fig. 3 thereof, there is

illustrated a general block diagram of the signal processing implementation of the present invention. The received RF signals from the two antennas 130 and 135 is sequentially sampled by a single pole double through (SPDT) switch 150 which is used as a multiplexer. The switching rate ("SR") of the SPDT switch 150 should be at least twice the Nyquist required sampling rate ("Fs") for the received signal bandwidth. Since, the Nyquist sampling rate is greater than twice the signal bandwidth, the SPDT switch 150 sampling rate will be greater than four times bandwidth, e.g. $F_s > 2 \cdot BW$ signal and $SR > 2 \cdot F_s$, where BW signal is the signal bandwidth. Generally SR will be selected to be N times F_s for N antennas.

The output signal of the SPDT is a multiplexed single analog (RF) signal, which comprises the RF signals received by the two antennas. The bandwidth of the multiplex signal at the output of the SPDT switch 150 is half of the switching rate ($SR/2$). This bandwidth is more than twice the bandwidth of the input RF signal for two antennas. This bandwidth requires that the rest of the receiving chain, e.g. the downconverter, has to support this higher bandwidth in order to enable de-multiplexing of the two signals at a later point.

The multiplexed signal is down converted by down converter 155 to an IF or baseband signal. The down converted signal is provided to an analog to digital converter 165 (A/D) which in turn provides the digital signal. The digital signal is demodulated and processed at the signal processor unit 160. The analog to digital converter 165 can be implemented externally to the signal processor 160 unit, or internally on the same chip.

At the signal processor 160 the digital signal is demultiplexed by demultiplexer 170 and received at a dual channel receiver 175. The signal at each of the channels of the dual channel receiver is related to the signal at each of the antennas 130 135. The dual channel receiver 175 also provides a control signal to the SPDT switch 150 that synchronizes the switching rate SR with operation of the clocks of the dual channel receiver 175.

The dual channel receiver 175 can be configured to implement various functions, including simply providing multiple data signals, if each of the antennas 130 and 135 is positioned to receive a different communication signal. In addition, antenna diversity or beam forming can be fully accomplished at the signal processor as described with respect to Fig. 4 and Fig 5.

It is presently preferred that a low noise amplifier 140 or 145 is used before the SPDT 150 for each of the antenna 130 and 135, to amplify the received signal and to maintain a maximum signal to noise ratio in the receiver.

5 A band pass filter (BPF) is included after each of the LNA 140 and 145. This BPF rejects out of band signals. The sampling rate SR at the SPDT 150 should be at least twice the rejection bandwidth of this BPF, in order to reduce interference from adjacent channels.

10 Although other combinations of components may be utilized, in one preferred embodiment, the LNAs 140, 145 and SPDT 150 are constructed on a single active RF chip. The band pass filter (BPF) between the LNA and the SPDT switch, can be implemented either on chip or externally.

15 The architecture of Fig. 3 was described above for a receiver with two antennas. The same concept can be used with higher number of antenna by multiplexing the RF input signal and demultiplexing at the signal processor. In this case, for receiving with N antennas the SPDT switch 150
20 will be replaced by a SPNT (N input and single output). For receiving with N antennas the switching rate will be the number of antennas multiplied by the required sampling

rate per each antenna signal, e.g. $SR=N*FS$ where N is the number of antennas, and $FS>2*B_{\text{signal}}$.

The same concept can be use for generating a multiplexed signal from several antennas with separate transmitters if their symbol rates are synchronized. This can be implemented as an example in point to multi point systems when the upstream symbol rate can be locked onto the common downstream symbol rate. In this case, after demultiplexing the signal in the signal processor 160, parallel demodulator blocks can be implemented in the same signal processor, e.g. signal processor 160. Such an architecture depends only on the signal processing capability of the signal processor, and can easily be achieved for low bit rate signals.

The cost reduction in the RF equipment allowed by the present invention is easily seen by comparing the common block diagrams of Fig 1 and Fig 2 with the presently preferred embodiment depicted in the block diagram of Fig 3 due to the reduced number of components. For example, the known antenna diversity block diagram of Fig. 1 utilizes two down converters 25 and 30, versus one for the present invention. The cost savings over the system of Fig 2 results from the elimination of the beam forming RF module

80, which includes complicated RF phase and amplitude controls.

Referring to Fig 4, a presently preferred configuration of the signal processor 160 utilized for beam forming is depicted. The analog multiplexed signal either at IF or baseband frequency, is converted to a digital signal by the A/D 200. The digital signal is demultiplexed into a stream of two separate digital data streams, each of which is from a separate antenna. Each of the digital data streams is filtered by the appropriate digital Band Pass Filter (BPF) 210 and 215, for a bandwidth equal to the transmitted bandwidth. Since, the digital signals have the same amplitude and phases as the RF signals received at each of the front antennas, but have a much lower frequency carrier, e.g. IF or baseband compared to RF, a vector summation of these digital signals is equivalent to a vector summation of the RF. Therefore, controlling the amplitude and phase of these digital signals is equivalent to the same processing of the RF.

The two data streams are delivered to the Beam Forming and Demodulator block 225, and also to the Channel Estimation block 220. The beam forming processing is accomplished by summation of the two digital signals after

amplitude balancing and phase shifting. The phase shifting enables control of the beam direction, as in a conventional RF beam forming process. By using more than two antennas, the beam can be optimized to have a spatial notch, to reject interference, as in conventional phased array techniques. The control of the phase and amplitude is accomplished by the channel estimator 220. The channel estimator controls the relative phase shift of the two data stream according to known algorithms that implements minimization of the data errors at the demodulator and decoder output.

The signal after the summation is demodulated as a regular signal, and the received data is decoded at the decoder 240 to deliver the final data output. During demodulation processing the carrier frequency and the sampling frequency F_s are extracted. From the extracted sampling frequency the demodulator acquires and provides a signal to synchronize the Sync SR To SPDT 230, and the Sync SR Delay 235. The Sync SR To SPDT 230 is the double sampling rate switching clock of the SPDT switch 150. The Sync SR Delay 235 is the corresponding delayed synchronized clock for the de-multiplexer 205. These two synchronization signals are at the same frequency, but the

timing signal provided to the demodulator is delayed to compensate for the down converter and filter delays between the RF and the output of the A/D 200.

Fig 5 a presently preferred configuration of the
5 signal processor 160 for the performance of antenna diversity. The analog multiplexed signal either at IF or baseband frequency is converted to a digital signal by A/D 250. As was describe with respect to Fig. 4 above, this digital signal is de-multiplexed into a stream of two
10 separate digital signals, each of them is related to a separate antenna by demultiplexer 235. Each of the digital data streams is then filtered to the transmitted bandwidth by the appropriate digital Band Pass Filter (BPF) 260 or 265. The two data streams are then demodulated and decoded
15 in parallel by demodulator decoders 270 and 275. The two demodulated data streams are delivered to the buffer 285, while the error information is delivered to the diversity controller 280. The diversity controller 280 selects the best packet data stream from the two demodulators according
20 to a minimum error criterion that is predetermined and based on the FEC. The selected data packet is the data output.

The architecture described with respect to Fig. 3 can be used with various modulation schemes, e.g. single carrier signals such as QAM, QPSK, BPSK or the like, as well as multiple carrier signals such as OFDM. In single
 5 carrier schemes, the demodulators used in the signal processor 160 will be the standard demodulator block for the modulation scheme.

For OFDM signals the band pass filters 210 and 215, and 260 and 265 are implemented by a FFT block which is a
 10 standard signal processing block. For OFDM type signals when each of the two data stream is split by the FFT block into multiple sub carriers data stream, the diversity scheme can be implemented by comparing the amplitude of each carrier and using the higher one for the demodulation
 15 process. This will significantly reduce the fading influence when it is not equally distributed on the signal bandwidth.

The beam forming processing of Fig. 4 can also be implemented to OFDM signals. For OFDM type signals each of
 20 the two data stream is split by the FFT block into multiple sub carriers data stream. The beam forming process 225 can be done separately on pairs of the same subcarrier from the two channels. This processing has the advantage of cancel

estimation optimization per sub carrier, which has a higher improvement gain.

5 The signal processor 160 is currently preferred to be an integrated circuit, but can also be one or more separate elements. Further, even though Figs. 4 and 5 depict the signal processor 160 as including A/D functionality, it should be noted that the A/D functionality may be separate from signal processor 160.

10 The present invention may be conveniently implemented using a conventional general purpose or a specialized digital computer or microprocessor programmed according to the teachings of the present disclosure, as will be apparent to those skilled in the computer art.

15 Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will be apparent to those skilled in the software art. The invention may also be implemented by the preparation of application specific integrated circuits or by interconnecting an appropriate network of conventional
20 component circuits, as will be readily apparent to those skilled in the art.

The present invention includes a computer program product which is a storage medium (media) having

instructions stored thereon/in which can be used to control, or cause, a computer to perform any of the processes of the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disks, mini disks (MD's), optical discs, DVD, CD-ROMS, micro-drive, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, DRAMs, VRAMs, flash memory devices (including flash cards), magnetic or optical cards, nanosystems (including molecular memory ICs), RAID devices, remote data storage/archive/warehousing, or any type of media or device suitable for storing instructions and/or data.

Stored on any one of the computer readable medium (media), the present invention includes software for controlling both the hardware of the general purpose/specialized computer or microprocessor, and for enabling the computer or microprocessor to interact with a human user or other mechanism utilizing the results of the present invention. Such software may include, but is not limited to, device drivers, operating systems, and user applications. Ultimately, such computer readable media further includes software for performing the present invention, as described above.

Included in the programming (software) of the general/specialized computer or microprocessor are software modules for implementing the teachings of the present invention, including, but not limited to, multiplexing RF
5 or other communication signals, downconverting the multiplexed signals, transporting the multiplexed signals through a single chain (e.g., RF chain, optic chain, etc.), de-multiplexing and using each signals in a related (or different) applications, and the display, storage, or
10 communication of results according to the processes of the present invention.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within
15 the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.